REMARKS

After entry of this amendment, claims 1-7, 9-15, 17-22, 25-26, 28, 31-32, 34, 37, and 39 are pending. In the present Office Action, claims 1-7, 9-15, 17-22, 25-26, 28, 31-32, 34, 37, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Glew et al., U.S. Patent No. 5,721,857 ("Glew"). Applicant respectfully traverses this rejection and requests reconsideration.

Claims 1-7 and 9-15

Applicant respectfully submits that each of claims 1-7 and 9-15 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the execution core is configured, in response to a system call instruction, to conditionally update a given flag of the plurality of flags dependent on a respective indication of the plurality of indications in the mask; and a second register configured to store the plurality of flags, wherein the execution core is configured to store the updated plurality of flags in the second register in response to the system call instruction".

The present Office Action alleges that the mask is taught by the exception mask bits in Glew's control register and that the plurality of flags are taught by the exception flags in Glew's status register (see, e.g., Office Action, page 3). However, Glew teaches "Bits 0-5 indicate whether the FPU *has detected* one of six possible *exception conditions* since these status bits were last cleared or reset." (Glew, col. 1, lines 56-58) Additionally, Glew teaches "Each of the six classes of numeric exceptions listed above has a corresponding flag bit in the FPU status word and a mask bit in the FPU control word. If an exception is masked (mask bit=1), the processor takes an appropriate default action and continues with the computation. If the exception is unmasked, a macro-code exception handler is invoked immediately before execution of the next WAIT or non-control FP instruction." (Glew, col. 2, lines 59-66). Thus, Glew's exception mask bits control whether or not an exception handler is invoked when an exception is detected. However, Glew's exception mask bits DO NOT control whether or not the exception flag bits are updated in the status register. Rather, these bits are updated if the FPU has

detected the exception condition, whether or not the exception handler is invoked.

Accordingly, Glew does not teach or suggest "the execution core is configured, in response to a system call instruction, to conditionally update a given flag of the plurality of flags dependent on a respective indication of the plurality of indications in the mask". Glew's exception mask bits have NO EFFECT on whether or not Glew's exception flag bits are updated. They only control whether or not an exception hander is invoked in response to the exception condition.

Furthermore, the present Office Action alleges that Glew teaches a system call instruction at col. 3, lines 2-3. However, these teachings (in context) are: "the exception handler is invoked either through interrupt vector 16 (an operating system call that invokes the exception handler when NE=0) or through an external interrupt (when NE=0)" (Glew, col. 3, lines 1-4). The "operating system call" being referred to by Glew is an interrupt vector, which is not an instruction as alleged in the present Office Action. An instruction is an executable entity defined in the instruction set architecture implemented by a processor. An interrupt vector is not such an entity, but rather is a mechanism to determine the address of an exception handler. Thus, Glew's interrupt vector does not teach or suggest a system call instruction as recited in claim 1.

For at least the above stated reasons, Applicant submits that claim 1 is patentable over the cited art. Claims 2-7, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Claims 2-7 each recite additional combinations of features not taught or suggested in the cited art.

Claim 9 recites a combination of features including: "the processor is configured, in response to a system call instruction, to conditionally update a given flag of the plurality of flags dependent on a respective indication of the plurality of indications in the mask; and a second storage location configured to store the plurality of flags, wherein the processor is configured to store the updated plurality of flags in the second storage location in response to the system call instruction". The teachings of Glew, highlighted

above with regard to claim 1, are also alleged to teach the above highlighted features of claim 9. Applicant respectfully submits that Glew does not teach or suggest the above highlighted features of claim 9, either. For at least the above stated reasons, Applicant submits that claim 9 is patentable over the cited art. Claims 10-15, being dependent from claim 9, are similarly patentable over the cited art for at least the above stated reasons. Claims 10-15 each recite additional combinations of features not taught or suggested in the cited art.

Claims 17-21

Applicant respectfully submits that each of claims 17-21 recite combinations of features not taught or suggested in the cited art. For example, claim 17 recites a combination of features including: "conditionally updating a given flag of a plurality of flags dependent on a corresponding indication in a mask, wherein the mask comprises a plurality of indications, and wherein each of the plurality of indications corresponds to a respective flag of the plurality of flags and indicates whether or not the respective flag is updated in response to the system call instruction; and the processing further comprising storing the updated plurality of flags in a storage location configured to store the plurality of flags".

The teachings of Glew, highlighted above with regard to claim 1, are also alleged to teach "conditionally updating a given flag of a plurality of flags dependent on a corresponding indication in a mask...and... storing the updated plurality of flags in a storage location configured to store the plurality of flags". Applicant respectfully submits that Glew does not teach or suggest the combination of features recited in claim 17, either.

Furthermore, Glew's teachings regarding exception mask bits and exception flags does not teach or suggest "each of the plurality of indications corresponds to a respective flag of the plurality of flags and indicates whether or not the respective flag is updated in response to the system call instruction". As highlighted above, Glew's exception mask bits control whether or not an exception handler is invoked in response to an exception

condition, but not whether or not a corresponding exception flag is updated.

For at least the above stated reasons, Applicant submits that claim 17 is patentable over the cited art. Claims 18-21, being dependent from claim 17, are similarly patentable over the cited art for at least the above stated reasons. Claims 18-21 each recite additional combinations of features not taught or suggested in the cited art.

Claims 22, 25-26, 28, 31-32, 34, 37, and 39

Applicant respectfully submits that each of claims 22, 25-26, 28, 31-32, 34, 37, and 39 recites a combination of features not taught or suggested in the cited art. For example, claim 22 recites a combination of features including: "a register configured to store a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction".

The present Office Action alleges that Glew teaches the above highlighted features, referring to the same teachings highlighted above with regard to claim 1. As highlighted above, however, Glew's exception mask bits control whether or not an exception handler is invoked in response to an exception condition, but not whether or not a corresponding exception flag is updated. Thus, Glew's exception mask bits do not teach or suggest "a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction". Furthermore, Glew teaches "Bits 0-5 indicate whether the FPU has detected one of six possible exception conditions since these status bits were last cleared or reset." (Glew, col. 1, lines 56-58). Clearly, then, Glew's processor sets an exception flag to indicate that an exception condition has been detected. Accordingly, even if, *arguendo*, Glew's exception mask bits had an effect on the exception flags, they would control whether or not the exception flag bit was set or not changed. This would not teach or suggest "a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction".

For at least the above stated reasons, Applicant submits that claim 22 is patentable over the cited art. Claims 25-26, being dependent from claim 22, are similarly patentable over the cited art for at least the above stated reasons. Claims 25-26 each recite additional combinations of features not taught or suggested in the cited art.

Claim 28 recites a combination of features including: "a storage location configured to store a value that defines which flags of a plurality of flags are to be cleared in response to a system call instruction and which flags of the plurality of flags are to be preserved in response to the system call instruction". The teachings of Glew, highlighted above with regard to claims 1 and 22, are also alleged to teach the above highlighted features of claim 28. Applicant respectfully submits that Glew does not teach or suggest the above highlighted features of claim 28, either. For at least the above stated reasons, Applicant submits that claim 28 is patentable over the cited art. Claims 31-32, being dependent from claim 28, are similarly patentable over the cited art for at least the above stated reasons. Claims 31-32 each recite additional combinations of features not taught or suggested in the cited art.

Claim 34 recites a combination of features including: "a plurality of instructions which, when executed in response to a system call instruction, clear one or more selected flags of a plurality of flags and preserve one or more other flags of the plurality of flags responsive to a value in a storage location". The teachings of Glew, highlighted above with regard to claims 1 and 22, are also alleged to teach the above highlighted features of claim 34. Applicant respectfully submits that Glew does not teach or suggest the above highlighted features of claim 34, either. For at least the above stated reasons, Applicant submits that claim 34 is patentable over the cited art. Claims 37 and 39, being dependent from claim 34, are similarly patentable over the cited art for at least the above stated reasons. Claims 37 and 39 each recite additional combinations of features not taught or suggested in the cited art.

CONCLUSION

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-78200/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

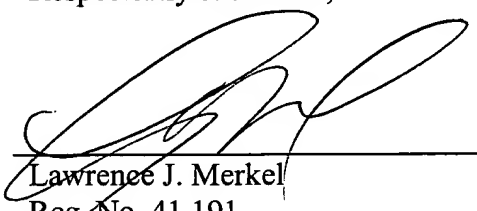
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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